Fabrication of ZnO thin film transistors by atomic force microscopy nanolithogrophy through zinc thin films

Jeff T. H. Tsai,[1,*] Ben H. B. Lee,[1] and Ming S. Yang[2]
[1]*Institute of Electro-optical Engineering, Tatung University, Taipei, Taiwan*
[2]*Research and Development Office, Tatung University, Taipei, Taiwan*
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Zinc oxide (ZnO) thin film transistors were fabricated by local anodic oxidation (LAO) of polycrystalline zinc film using an atomic force microscope (AFM). Nanometer-thin zinc film can be locally transformed into *p*-type zinc oxide by an anodic oxidation technique using an AFM at room temperature. With this fabrication process, we have fabricated a backgate, Schottky-barrier-contact type thin film ZnO transistor. This fabrication requires no semiconductor material to produce transistors, only conventional metal film. The fabrication creates active area and source/drain contacts through simple AFM oxidation, with no requirement for additional semiconductor thin film deposition and photolithography. A representative LAO thin film transistor fabricated in this study exhibited a field-effect mobility of 23.6 cm^2/V s, a peak transconductance of 15.8 μS, and an I_{on}/I_{off} ratio of 10^6. To the best of our knowledge, the mobility value attained for this LAO thin film transistor is higher than that of any previously reported amorphous-silicon-based thin film transistors. Its peak transconductance and I_{on}/I_{off} ratio are also enhanced compared with a backgate field-effect transistor with the same amorphous silicon channel as utilized in conventional thin film transistors.

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INTRODUCTION

Thin film transistors (TFTs) are widely used in conventional microelectronics. The best known application of TFTs is in liquid crystal displays and projectors, in which these transistors are embedded within the display panel, where they reduce crosstalk between pixels and improve image stability.[1] Basically, a thin film field-effect transistor requires an active layer of semiconductor material to form the controllable conduction channel. The most commonly used semiconductor material is an amorphous silicon (a-Si) thin film, which can be fabricated by a chemical vapor deposition technique.[2,3] Owing to its amorphous structure, a-Si carrier mobility tends to be low, in the range of 0.45–1 cm^2/V s.[4,5] To enhance the operation speed, polycrystalline silicon has been introduced into device fabrication. Laser scanning annealing,[6–8] rapid thermal annealing,[9,10] or mantel-induced crystallization approaches[11,12] have been utilized to transform amorphous silicon to polycrystalline silicon for enhancement of carrier mobility and device switching speed. However, these additional steps require tedious processing and precise temperature control.

Other metal-oxide semiconductor materials have been effective in TFT fabrications.[13] Zinc oxide (ZnO) has been considered a prime candidate for use in high performance transparent TFTs. As a semiconductor, ZnO has several favorable properties, including good transparency, high electron mobility, wide band gap, strong room-temperature luminescence, etc. ZnO also has a relatively large direct band gap of ~3.3 eV at room temperature.[14] Advantages associated with this large band gap include higher breakdown voltages, ability to sustain large electric fields, lower electronic noise, as well as high-temperature and high-powered operations.

Most ZnO has an *n*-type character, even in the absence of intentional doping. Nonstoichiometry is typically the origin of an *n*-type character; thus, reliable *p*-type doping of ZnO remains difficult. This problem originates from the low solubility of *p*-type dopants and from compensation by abundant *n*-type impurities.[15] Several research groups have managed to fabricate field-effect transistors using a ZnO nanorod as the active material. This wide-band-gap semiconductor nanorod has also been suggested as having potential uses in sensor, laser, and light-emitting-diode (LED) applications.[16]

As device size continues to shrink to fulfill the requirements of the latest microelectronic circuitry, the challenge of fabricating nanometer-sized transistors is now reliant on advances made in photolithography techniques. Although electron-beam lithography can be used to create nanometer scale patterns, this lithography tool is too expensive for routine use. AFM nanolithography is another emerging technology that has been praised for its cost-efficient potential to create features with dimension of tens of nanometer on various substrates.

Based on the spatial confinement of a chemical reaction within a nanometer-size region, AFM provides a region defined by a combination of the probe-sample surface geom-

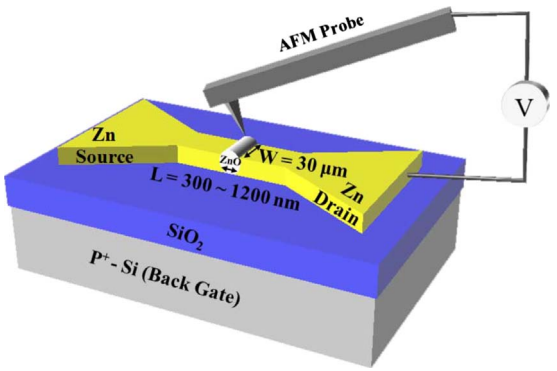

FIG. 1. (Color online) Schematic of the AFM nanolithography LAO ZnO TFT.

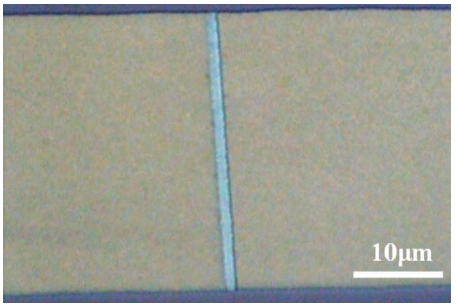

FIG. 2. (Color online) Optical image of the LAO ZnO transistor; a visible strip shows the transformation of Zn to ZnO.

etry and environmental humidity to form a water bridge. This water bridge acts as an electrolyte and limits the occurrence of the chemical reaction to a spatial confinement of nanometer size.[17] This technology is therefore able to perform sophisticated device fabrication, for example, a sensor can be fabricated with AFM oxidation technology using a single-crystalline silicon nanowire, to produce high electrical performance field-effect transistors with channel widths as small as 4 nm.[18] A side-gated silicon nanowire with a 30 nm air gap has also been demonstrated by AFM oxidation.[19] It is also possible to fabricate complex spintronic devices by AFM oxidation to create a nanomask for further etching processes that can create nanochannels.[20]

A key advantage to AFM nanolithography is that it can be performed in the open air at room temperature. In contrast, other oxide fabricating deposition processes need to take place within a high-vacuum apparatus at high temperatures. Thus, AFM local oxidization nanolithography could be a robust and handy room-temperature process for the simultaneous patterning of nanodesigns and transforming of metal to metal oxide. Therefore, AFM is suitable for fabricating solid-state devices on flexible substrates that require fabrication process in a relative low temperature, such as plastic films.

EXPERIMENT

In this paper, we report on an effective fabrication method for producing *p*-type ZnO TFTs. By combining fabrication with the AFM oxidation technique, we are able to create a prototype ZnO TFT, by transferring Zn to ZnO directly in the open air at room temperature. We oxidize part of the Zn thin film through a Zn stripe, which separates the metal stripe into a source/drain and joins it to the semiconductor (transformed ZnO), as shown in Fig. 1. This results in a backgate metal-oxide semiconductor (MOS) with a nonjunction Schottky barrier source-/drain-type TFT, which eventually prevents a short-channel effect.[21] Fabricating this type of a ZnO TFT by direct transformation of Zn into ZnO creates a device that exhibits characteristics of high performance and low contact resistance.

Conventional photolithography was applied to a highly doped p^+ silicon (100) wafer coated with a thermal growth silicon-dioxide thin film. Several stripes were then patterned using AZ 5214E photoresist. The bar pattern is 30 μm in width, 150 μm in length, and both ends have large visible patterns for use as probing pads. Zinc film was then deposited on this patterned substrate by a magnetron sputtering deposition system, using a Zn target of 99.99% purity at a base pressure of 10^{-7} torr at room temperature. The deposition time was 35 s. This provided a continuous Zn film at an average thickness of 17 nm. This step was followed by a lift-off process consisting of bathing the substrate in a photoresist stripper to remove any unwanted area. The result was a Zn line pattern. The substrate was then annealed at 200 °C in a vacuum furnace to smooth the surface of the polycrystalline Zn film.

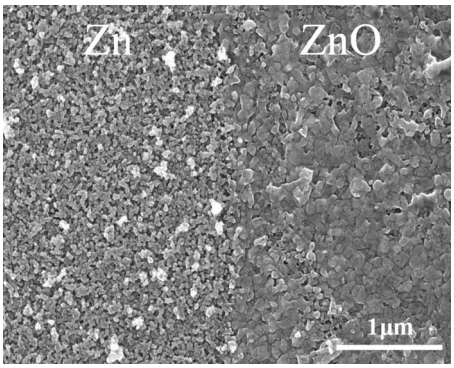

FIG. 3. SEM micrograph showing the part of transistor near the source of the active area. After LAO, a Zn/ZnO boundary was observed.

An AFM (Digital instrument NS3a controller with D3100 stage, Veeco Instruments Inc., U.S.A.) was employed to study the surface morphology and to perform the LAO process on the Zn stripes. We used a highly conductive silicon AFM stylus to perform the localized anodic oxidation, applying voltages of 4–12 V between the tip and the Zn by scanning the tip in contact mode. This experiment was performed in an environment at a relative humidity of 80%. With an optical microscope, a visible strip was clearly

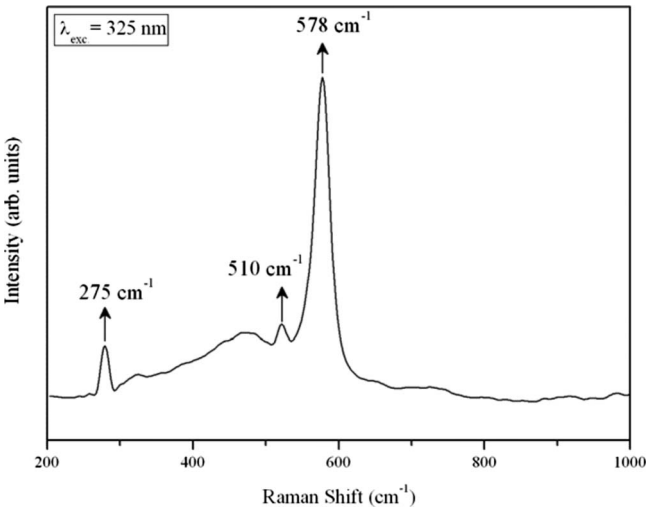

FIG. 4. The micro-Raman spectrum of ZnO films produced by AFM nanolithography. The peak at 578 cm^{-1} is attributed to the A_1 (LO) mode of ZnO. 275 and 510 cm^{-1} are the Raman features related to nitrogen concentration in ZnO films.

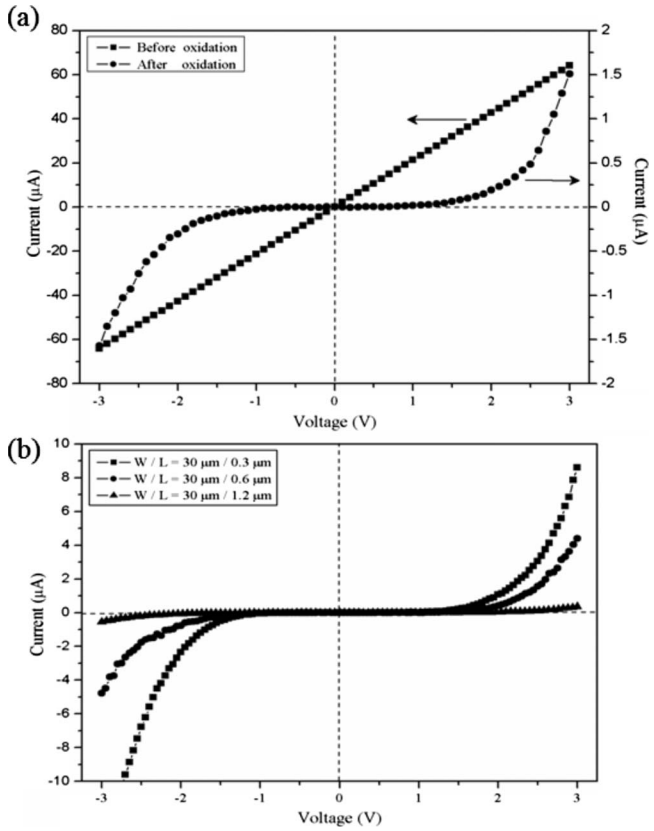

FIG. 5. (a) Comparison of *I-V* curves before and after LAO. The source/drain conduction shows Ohmic and back-to-back diode characteristics. (b) Source/drain conduction currents are limited by the channel length *L*.

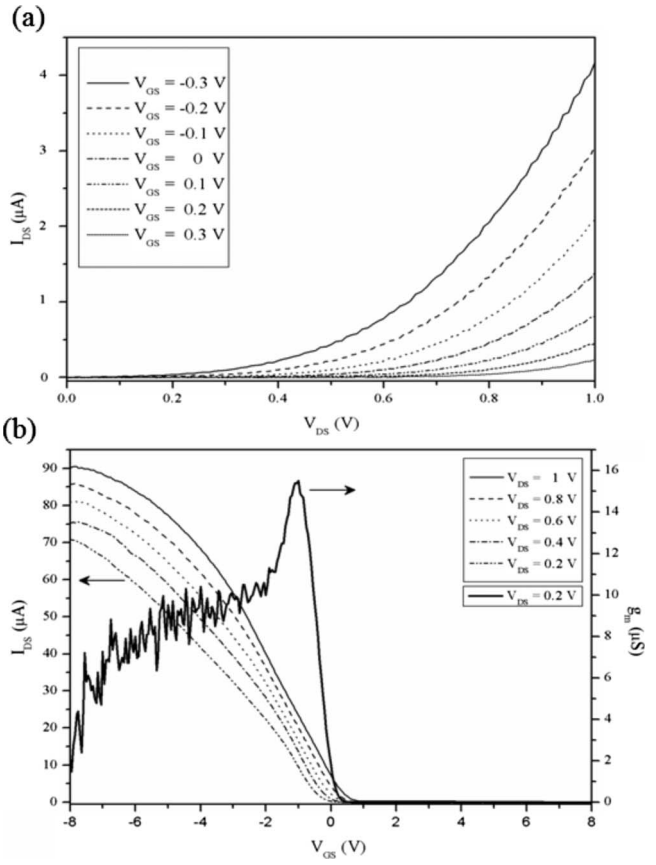

FIG. 6. (a) The drain transfer *I-V* characteristics of the backgate LAO ZnO TFT. I_{DS} to V_{DS} characteristics for V_{GS} values ranging from −0.3 to +0.3 V. (b) The gate transfer characteristics obtained from the LAO ZnO TFT. The I_{DS} vs V_{GS} characteristics for V_{DS} values ranging from 0.2 to 1 V; the transconductance g_m curves obtained from the LAO ZnO TFT at V_{DS}=0.2 V is included.

formed through the Zn stripe, as shown in Fig. 2. The AFM LAO ZnO shows multiple colors under white light at different oxidation voltages.[22] A scanning electron microscopy (SEM) image of this local oxidized boundary is shown in Fig. 3. In this case, the grain size of the zinc polycrystalline structure became enlarged when Zn was transformed to ZnO. This was confirmed by an AFM survey of the sample surface, which showed that the average grain size had increased.

RESULTS AND DISCUSSION

We analyzed this area using a micro-Raman system (Renishaw inVia) and found that a strong nanocrystalline ZnO Raman mode[23] appears at 578 cm^{-1}, showing that the transformation from Zn to ZnO has been completed (Fig. 4). We also observed Raman modes at 275 and 510 cm^{-1}, which relate to the nitrogen incorporated into the ZnO.[24] Tu *et al.*[25] have shown that additional nitrogen incorporated in the ZnO films can generate high-quality ZnO:N films, which were confirmed as *p*-type semiconductors by Hall measurement. Therefore nitrogen is a *p*-type dopant for ZnO.

A tunneling diode has been demonstrated using AFM nanolithography.[26] A thin tunneling barrier of nanometer scale was created by local oxidation of metals. The *I-V* characteristic deviates from Ohm's law when the device is measured at cryogenic temperature. In contrast to the operating principal of the tunneling device, we produced semiconductor material from metal by AFM oxidation. For the conductivity of our device at room temperature through the source/drain, the *I-V* characteristics exhibited a back-to-back diode characteristic after the LAO process [Fig. 5(a)]. This demonstrates that the AFM LAO has completely converted the metal into a semiconductor and has naturally formed two Schottky contacts. The width of the LAO area can be controlled by the AFM scanning rate. We characterized the devices at 300 nm, 600 nm, and 1.2 μm and the *I-V* characterization is shown in Fig. 5(b).

Our LAO backgate TFT can be realized by applying gate voltages (V_{GS}) to the substrate. The typical output and transfer characteristics obtained from a representative LAO ZnO FET with a channel length of 300 nm (LAO regime) and channel width of 30 μm (line width of Zn stripe) are shown in Fig. 6(a). The family of I_{DS}-V_{DS} curves shows that the drain current increases with increasing drain voltage. The slope of the I_{DS}-V_{DS} curve also increases dramatically as the gate voltage V_{GS} increases from 0.3 to −0.3 V.

The I_{DS}-V_{GS} curves in Fig. 6(b) show that I_{DS} first increases and then slightly saturates as V_{GS} increases from −1 to −8 V. I_{DS} is totally depleted in the V_{GS} range from 1 to 8 V. These characteristics reveal that the device is a *p*-type

depletion mode FET. The I_{DS}-V_{GS} transfer and transconductance curves obtained for the representative LAO transistor at $V_{DS}=0.2$ V are plotted in Fig. 6(b). The I_{DS}-V_{GS} transfer curve demonstrates an I_{on}/I_{off} ratio of 10^6, which is comparable to values previously reported for nanowire-based FETs. The transconductance curve reveals a peak transconductance (g_m) of 15.8 μS at $V_{GS}=-1.1$ V [Fig. 6(b)]; for comparison, a corresponding I_{DS}-V_{GS} curve is included in the same figure. The threshold voltage obtained from the I_{DS}-V_{GS} transfer curve is 0.3 V. The subthreshold slope obtained from the I_{DS}-V_{GS} curves at $V_{DS}=0.2$ V yields a value of 227 mV/decade. To calculate the effective mobility, the capacitance of the gate dielectrics for our LAO ZnO TFT is estimated as follows. The capacitance C_i is estimated to be 3.1 fF on the basis of the formula $C_i=\varepsilon_0\varepsilon_r A/d$, where ε_r is the dielectric constant of SiO_2 (3.9), d is the thickness of the gate oxide (100 nm), and A is the active area derived from the gate length L (300 nm) multiplied by the gate width W (30 μm). In this TFT, the channel length is defined by the LAO area, which may be considered as the gate length, since it is a backgated structure. The formula used for obtaining the field-effect mobility (μ_{FE}) can be derived from the formula utilized for conventional planar MOS FETs (Ref. 21) by the maximum of transconductance, $g_m=(W/L)\mu_{FE}C_iV_D$. Here, the mobility is estimated to be 23.6 $cm^2/(V\,s)$ at $V_{DS}=0.2$ V, on the basis of the experimental result of $g_m=15.8$ μS.

CONCLUSION

In conclusion, we successfully fabricated LAO TFTs with channels created by an AFM oxidation conversion of Zn to *p*-type ZnO. Our prototype LAO device exhibits remarkably enhanced electrical characteristics when compared with conventional backgate TFTs. The peak transconductance can reach 15.8 μS, a field-effect mobility of 23.6 $cm^2/(V\,s)$ is achieved, and the I_{on}/I_{off} ratio can approach 10^6. There is no thermal process required in the use of the LAO by an AFM for the fabrication of practical transistors. Therefore, this approach is suitable for fabricating TFTs on low-cost flexible substrates, such as plastic film. The observed enhancement of the electrical characteristics is mostly attributed to the LAO process, which forms a smooth transition from the metal contact site (Zn) to the semiconductor site (ZnO). This structure eventually prevents the short-channel effect and omits the tedious source/drain implantation procedure.

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*thtsai@ttu.edu.tw

[1] D. J. R. Cristaldi, S. Pennisi, and F. Pulvirenti, *Liquid Crystal Display Drivers: Techniques and Circuits* (Springer, New York, 2009).
[2] E. Kinsbron, M. Sternheim, and R. Knoell, Appl. Phys. Lett. **42**, 835 (1983).
[3] S. K. Kim, Y. J. Choi, K. S. Cho, and J. Jang, J. Appl. Phys. **84**, 4006 (1998).
[4] H. Gleskova and S. Wagner, Appl. Phys. Lett. **79**, 3347 (2001).
[5] J. M. Hvam and M. H. Brodsky, Phys. Rev. Lett. **46**, 371 (1981).
[6] M. O. Thompson, G. J. Galvin, J. W. Mayer, P. S. Peercy, J. M. Poate, D. C. Jacobson, A. G. Cullis, and N. G. Chew, Phys. Rev. Lett. **52**, 2360 (1984).
[7] M. Miyasaka and J. Stoemenos, J. Appl. Phys. **86**, 5556 (1999).
[8] K. Sera, F. Okumura, H. Uchida, S. Itoh, S. Kaneko, and K. Hotta, IEEE Trans. Electron Devices **36**, 2868 (1989).
[9] R. Kakkad, J. Smith, W. S. Lau, S. J. Fonash, and R. Kerns, J. Appl. Phys. **65**, 2069 (1989).
[10] Gang Liu and S. J. Fonash, Appl. Phys. Lett. **55**, 660 (1989).
[11] M. A. T. Izmajlowicz, A. J. Flewitt, W. I. Milne, and N. A. Morrison, J. Appl. Phys. **94**, 7535 (2003).
[12] C.-W. Lin, P.-A. Chang, and Y.-S. Lee, J. Mater. Sci.: Mater. Electron. **18**, 475 (2007).
[13] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, Nature (London) **432**, 488 (2004).
[14] V. Srikant and D. R. Clarke, J. Appl. Phys. **83**, 5447 (1998).
[15] F. Tuomisto, V. Ranki, K. Saarinen, and D. C. Look, Phys. Rev. Lett. **91**, 205502 (2003).
[16] D.-K. Hwang, S.-H. Kang, J.-H. Lim, E.-J. Yang, J.-Y. Oh, J.-H. Yang, and S.-J. Park, Appl. Phys. Lett. **86**, 222101 (2005).
[17] R. Garcia, R. V. Martínez, and J. Martinez, Chem. Soc. Rev. **35**, 29 (2006).
[18] J. Martinez, R. V. Martínez, and R. Garcia, Nano Lett. **8**, 3636 (2008).
[19] N. Clément, D. Tonneau, H. Dallaporta, V. Bouchiat, D. Fraboulet, D. Mariole, J. Gautier, and V. Safarov, Physica E (Amsterdam) **13**, 999 (2002).
[20] L. Pellegrino, Y. Yanagisawa, M. Ishikawa, T. Matsumoto, H. Tanaka, and T. Kawai, Adv. Mater. (Weinheim, Ger.) **18**, 3099 (2006).
[21] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices* (John Wiley & Sons, New York, 2007).
[22] J.-S. Hwang, L.-W. Chen, T.-C. Chen, C.-W. Kuo, Z.-S. Hu, T.-R. Tsai, Y.-J. Wu, T.-Y. Lin, Y.-Y. Jhuo, C.-Y. Cheng, C.-M. Lin, and Y.-H. Liu, Nanotechnology **20**, 055302 (2009).
[23] L. Bergman, X. B. Chen, J. Huso, J. L. Morrison, and H. Hoeck, J. Appl. Phys. **98**, 093507 (2005).
[24] A. Kaschner, U. Haboeck, Martin Strassburg, Matthias Strassburg, G. Kaczmarczyk, A. Hoffmann, C. Thomsen, A. Zeuner, H. R. Alves, D. M. Hofmann, and B. K. Meyer, Appl. Phys. Lett. **80**, 1909 (2002).
[25] M.-L. Tu, Y.-K. Su, and C.-Y. Ma, J. Appl. Phys. **100**, 053705 (2006).
[26] J. I. Shirakashi and Y. Takemura, IEEE Trans. Magn. **40**, 2640 (2004).